HENP 2019 Advance Program

9:00-10:00 Keynote
"Beyond Autoregressive Neural Sequence Models," Prof. Kyunghyun Cho, NYU/Facebook AI Research.

10:00-10:30 Coffee break & poster

10:30 - 12:30 Session 1
"Sub-Milliwatt and Sub-Microwatt Hardware Architecture for Embedded Intelligent Systems," Prof. Mingoo Seok, Columbia University.
"Off-chip-memory-traffic-aware Neural Network Architecture Design," Prof. Youn-Long Lin, National Tsing Hua University.
"Learning to Quantize Deep Networks by Optimizing Quantization Intervals with Task Loss," Dr. Jae-Joon Han, Samsung Advanced Institute of Technology.

12:30 - 13:30 Lunch & poster

13:30 - 15:00 Session 2
"Security of Intelligent Application," Prof. Gabriela Nicolescu, Polytechnique Montréal.
"Unsafe optimizations for efficient on-chip inference via voltage tuning, eNVMs, and sparse encoding," Dr. Brandon Reagen, NYU/Facebook.
"Algorithm/Hardware Co-design for Energy/Area efficient In-Memory Neural Network Computing," Prof. Jae-joon Kim, POSTECH.

15:00 - 15:30 Coffee break & poster

15:30 - 17:00 Session 3 and poster
"From Matrix to Tensor: Algorithm and Hardware Co-design for Energy-efficient Deep Learning," Prof. Bo Yuan, Rutger University.
"From 7,000X model compression to 100X acceleration: Achieving real-time execution of ALL DNNs on mobile devices," Prof. Yanzhi Wang, Northeastern University.
*Poster continues by 5pm

Posters
"A Desirable Sparsity Dimension for Real-time Acceleration – From Algorithm to Framework," Xiaolong Ma, Northeastern University, and College of William and Mary.
"Hardware Architecture for On-sensor Neural Network Computing," Yuki Arikawa, NTT Device Technology Labs.
"High Throughput CNN Inference on Heterogeneous MPSoCs," Siqi Wang, National University of Singapore.
"A Memory-Centric Hyperdimensional Computing with Stochastic Training," Mohsen Imani, UC San Diego.
"Digital-based Processing In-Memory for Acceleration of Unsupervised Learning," Mohsen Imani, UC San Diego.
"Input-Splitting of Large Neural Networks for Power-Efficient Accelerator with Resistive Crossbar Memory Array," Jae-Joon Kim, POSTECH.